# DEMODULATOR FOR COMPACT DISC

# SAA7010

## GENERAL DESCRIPTION

The SAA7010 demodulates and decodes the pulse code modulated input signal into digital data for the Compact Disc Digital Audio system. A 4,3 MHz (typical) clock locked to the disc rate is also produced.

### Features

- Phase-locked loop clock regenerator with frequency detector for locking
- High-frequency level detector with adaptive slicer for input data
- Built-in drop-out detector to prevent error propagation in adaptive slicer
- Outputs to subcoding microprocessor
- Fully protected timing synchronization to incoming data



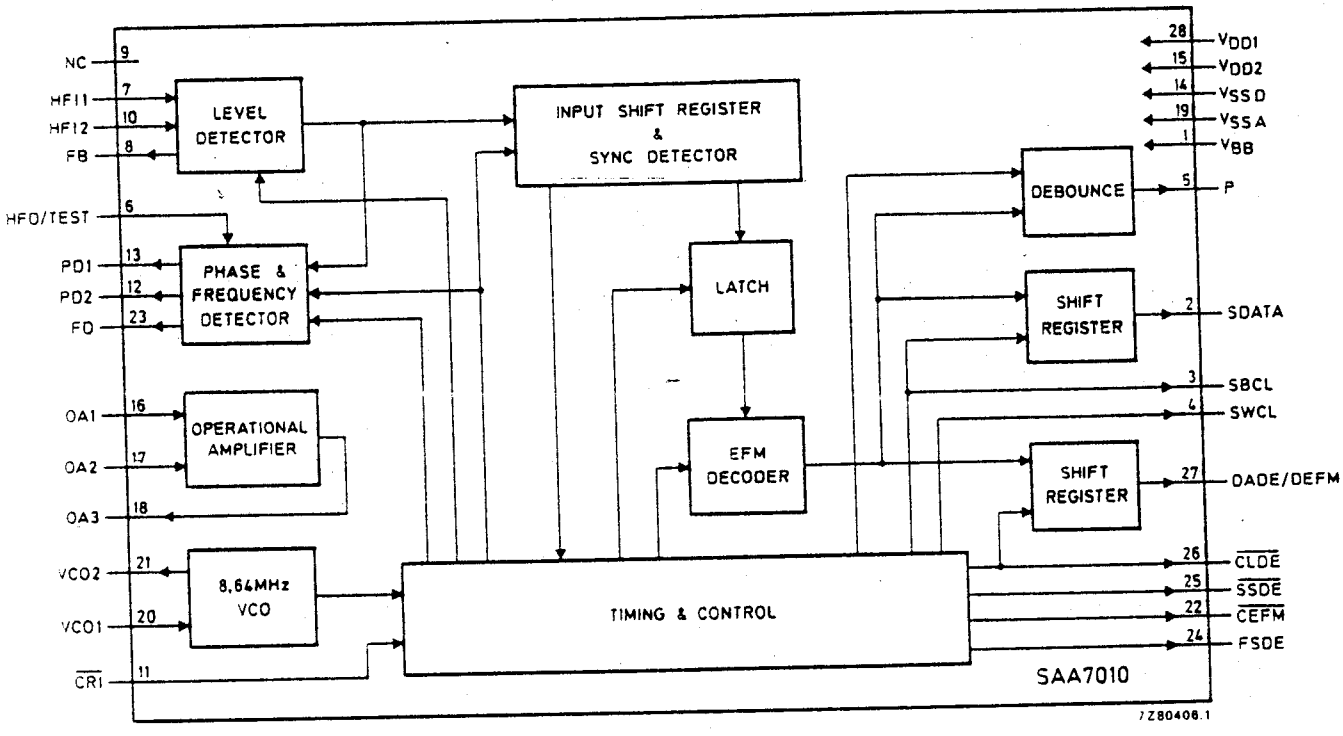


Fig. 1 Block diagram.

## PACKAGE OUTLINE

28-lead DIL; package (SOT-117).

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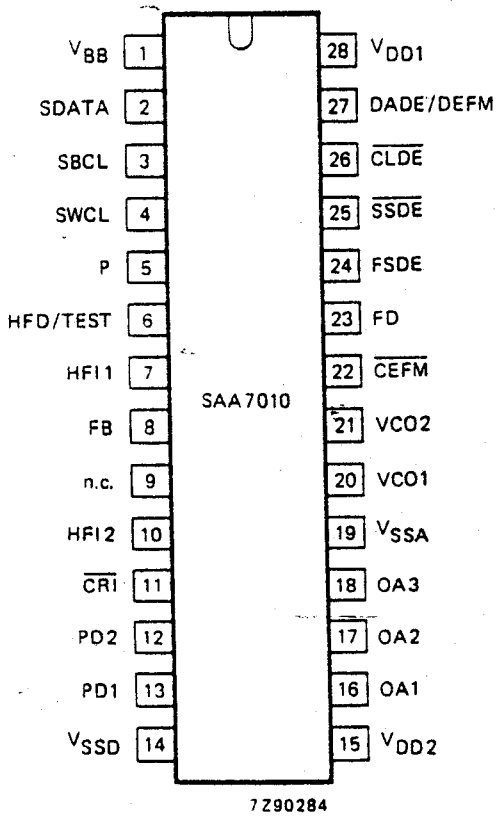


Fig. 2 Pinning diagram.

## PINNING

| | | |
|---|---|---|
| 1 | $V_{BB}$ | back bias supply |
| 2 | SDATA | subcoding data output |
| 3 | SBCL | subcoding bit clock output |
| 4 | SWCL | subcoding word clock output |
| 5 | P | subcoding pause bit output |
| 6 | HFD/TEST | high-frequency detector input in normal operation. Selects test mode when at $V_{DD2}$ |
| 7 | HFI1 | level detector input |
| 8 | FB | current feedback from level detector |
| 9 | n.c. | not connected |
| 10 | HFI2 | alternative input to level detector |
| 11 | $\overline{CRI}$ | counter reset inhibit input |
| 12 | PD2 | phase detector reference output |
| 13 | PD1 | phase detector signal output |
| 14 | $V_{SSD}$ | digital ground |
| 15 | $V_{DD2}$ | + 12 V supply |
| 16 | OA1 | operational amplifier non-inverting input |
| 17 | OA2 | operational amplifier inverting input |
| 18 | OA3 | operational amplifier source-follower output |
| 19 | $V_{SSA}$ | analogue ground |
| 20 | VCO1 | voltage-controlled oscillator amplifier input |
| 21 | VCO2 | voltage-controlled oscillator amplifier output |
| 22 | $\overline{CEFM}$ | 4,3218 MHz clock output |
| 23 | FD | frequency detector output |
| 24 | FSDE | frame sync signal output |
| 25 | $\overline{SSDE}$ | symbol sync signal output |
| 26 | $\overline{CLDE}$ | data bit clock output |
| 27 | DADE/DEFM | serial data output/EFM digital output: selection determined by level at pin 11 |
| 28 | $V_{DD1}$ | + 5 V supply |

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## FUNCTIONAL DESCRIPTION

The SAA7010 demodulator forms the front-end of the Compact Disc Digital Audio system, supplying demodulated data and timing signals to the error corrector (SAA7020) and to the subcoding microprocessor.

The detected signal from the disc is amplified and filtered externally and then converted to a digital signal via the level detector. The level detector is an adaptive data slicer which relies on the nature of the modulation system to determine the optimum slicing level.

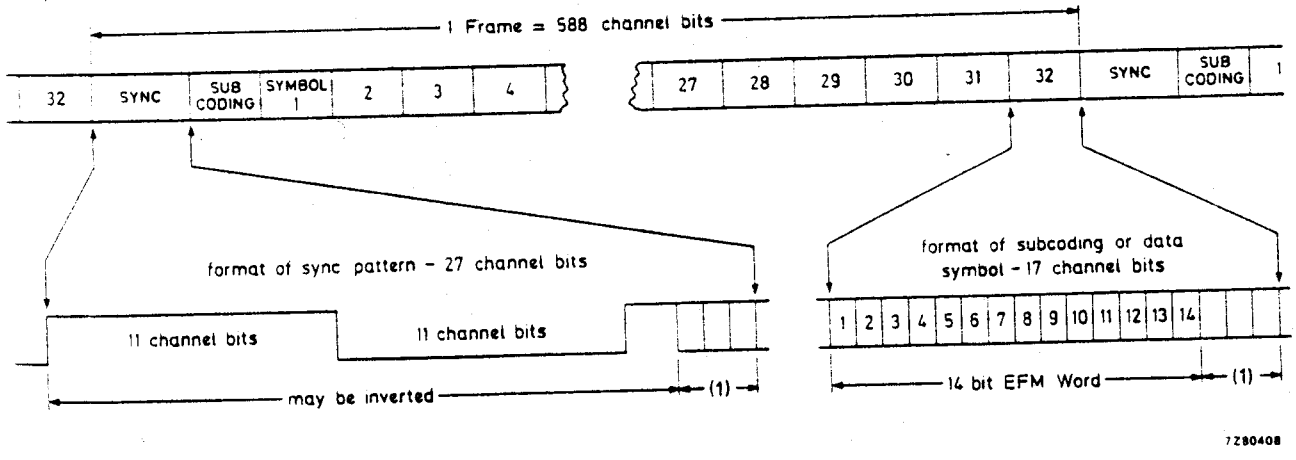
A frequency detector and a phase detector provide the coarse and fine control signals for the phase-locked loop (PLL) system. The loop gain is supplied by an internal operational amplifier which drives a voltage-controlled oscillator (VCO) running at twice the input data rate (typically 8,6436 MHz). The VCO output is divided by two by a clock generator in the timing and control circuits and the resulting output is used to clock the input shift register and the timing chain. This clock signal completes the PLL loop when it is compared with the incoming data in the phase detector.



After phase detection the data is clocked into the 23-bit input shift register which then detects the frame sync pattern. Within the timing and control circuits are minimum and maximum data length detectors which provide frequency limit signals for the frequency detector.

Also within the timing and control circuits are two divide-by-588 counters, one master and one slave, two divide-by-17 symbol rate counters and a lock indication counter. The frame sync signal is used to reset the divide-by-588 slave counter. This counter and one divide-by-17 symbol rate counter supply timing signals for clocking the EFM (eight-to-fourteen modulation) decoder and the subcoding output circuits. The data is read from the input shift register in 14-bit symbols which are first latched and then decoded into 8-bit data words. The subcoding part of the data consists of one word per frame (Fig. 3), so the output SDATA comprises a burst of 8 data bits accompanied by a 2,1906 MHz clock burst signal SBCL (Fig. 4). One bit of this subcoding output data is replaced by a subcoding frame sync bit which is decoded from one of two special EFM codes. The displaced bit (the pause (P) bit) is latched to its own output via a debounce circuit to remove erroneous changes.

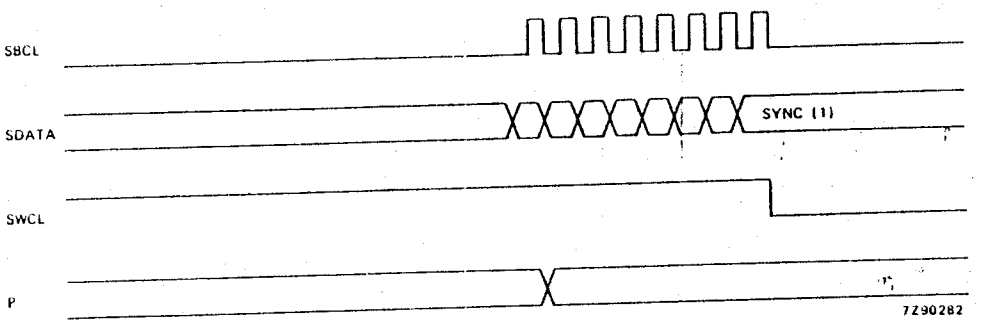
The divide-by-588 slave counter also provides a sync coincidence pulse which occurs when two detected sync pulses are precisely one frame apart (588 clock cycles). The sync coincidence pulse is used to reset the lock indication counter and disable the FD output from the frequency detector. If the system goes out of lock, the sync pulses cease and the lock indication counter counts frame periods. After 63 frame periods with no sync coincidence pulse, the lock indication counter enables the frequency detector output.




(1) Merging and low frequency suppression bits.

Fig. 3 Data input signal.

## FUNCTIONAL DESCRIPTION (continued)




(1) The sync bit is LOW when a subcoding sync word is detected.

Fig. 4 Typical subcoding waveform outputs.

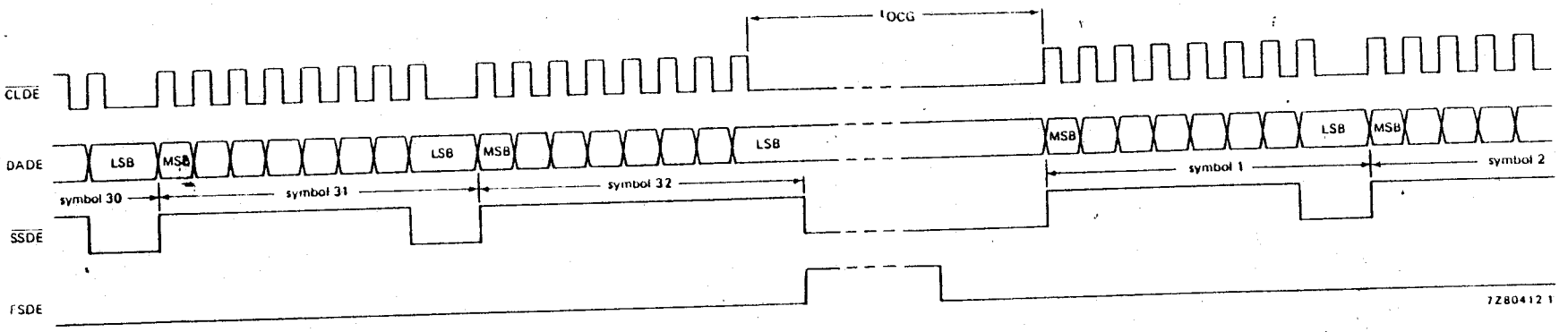



Fig. 5 Typical waveform outputs to SAA7020.

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## FUNCTIONAL DESCRIPTION (continued)

A delayed version of the sync coincidence pulse resets the divide-by-588 master counter. This counter is reset only by coincident sync pulses or sync pulses which occur during a predetermined 'window' at the start of each frame and is therefore protected from accidental reset by erroneous sync patterns. The window is wide enough to allow PLL bit-slips but narrow enough to avoid false sync signals generated by corrupt data. The divide-by-588 master counter may be allowed to free-run by taking $\overline{CRI}$ input (pin 11) LOW to inhibit the reset signal.

The divide-by-588 master counter and the second divide-by-17 symbol rate counter are used to time the data and clock outputs to the error corrector SAA7020 (Fig. 5). In this way, even if the data has been corrupted, the timing signals will be correct and are only re-synchronized after a complete frame has been sent to SAA7020.

The data output to SAA7020 comprises thirty-two 8-bit symbols per frame, with half-bit gaps between each symbol and a much longer gap during the frame sync period. It is this longer gap that changes in length when corrupt data upsets the timing system.

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### Pin functions

| pin no. | mnemonic | description |
|---|---|---|
| 1 | $V_{BB}$ | Back bias supply voltage: −2,5 V ± 20%. |
| 2 | SDATA | Subcoding data push-pull output. An 8-bit burst of data (including a 1-bit subcoding frame sync) is output serially once per frame coincident with SBCL. |
| 3 | SBCL | Subcoding bit clock push-pull output. An 8-bit burst clock, typically at 2,1609 MHz, is used to synchronize the subcoding data. |
| 4 | SWCL | Subcoding word clock push-pull output. A square-wave signal at data frame rate (7,35 kHz) used to synchronize the subcoding words and the pause (P) bit. |
| 5 | P | Subcoding pause bit push-pull output. This signal is derived from the encoded subcoding word and is used to indicate a music pause. A debounce circuit is incorporated to eliminate erroneous data. |
| 6 | HFD/TEST | External high-frequency detector input. When this signal is HIGH the frequency detector output (FD) and phase detector are enabled. When pin 6 is connected to $V_{DD2}$, the device enters TEST mode. |
| 7 | HFI1 | Level detector input. A signal of between 0,25 and 2,5 V (peak-to-peak value) is required to drive the level detector correctly. |
| 8 | FB | Current feedback from the level detector. |
| 9 | n.c. | Not connected. |
| 10 | HFI2 | Alternative input to the level detector. |
| 11 | $\overline{CRI}$ | Counter reset inhibit signal input. When LOW, this signal allows the divide-by-588 master counter to free-run and causes pin 27 output to be converted to DEFM. During power-up, pin 11 should be held HIGH for 10 ms. |
| 12 | PD2 | Phase detector reference signal, maximum impedance 10 kΩ. |
| 13 | PD1 | Phase detector output signal, maximum impedance 10 kΩ. The differential d.c. content of PD1 and PD2 signals is a measure of the phase difference between the data and the internal 4,3218 MHz clock. |

# DEMODULATOR FOR COMPACT DISC



| pin no. | mnemonic | description |
|---|---|---|
| 14 | $V_{SSD}$ | Digital ground. Main ground terminal. |
| 15 | $V_{DD2}$ | Positive supply voltage: + 12 V ± 10%. |
| 16 | OA1 | Operational amplifier non-inverting input. |
| 17 | OA2 | Operational amplifier inverting input. |
| 18 | OA3 | Operational amplifier source follower output. |
| 19 | $V_{SSA}$ | Analogue ground. Ground terminal for operational amplifier and VCO only. Connected internally to $V_{SSD}$ via a 25 Ω (nominal) resistor. |
| 20 | VCO1 | Voltage-controlled oscillator amplifier input. The amplifier is a simple inverter operating up to 10 MHz. Frequency control is achieved via an external tuned circuit using variable capacitance diodes. |
| 21 | VCO2 | Voltage-controlled oscillator amplifier output. The load for the inverting transistor may be turned off for test purposes by reducing $V_{DD2}$ to 0 V. |
| 22 | $\overline{\text{CEFM}}$ | Internal 4,3218 MHz clock generator push-pull output. |
| 23 | FD | Frequency detector three-state push-pull output. This output has a 1 kΩ |

## RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134);
$V_{SSA} = V_{SSD} = 0$ V.

| | | | |
|---|---|---|---|
| Supply voltage 1 range (pin 28) | $V_{DD1}$ | −0,3 to + 7,5 | V |
| Supply voltage 2 range (pin 15) | $V_{DD2}$ | −0,3 to + 15 | V |
| Back bias supply voltage range (pin 1) | $V_{BB}$ | −4 to + 0,3 | V |
| Input voltage range | $V_I$ | −0,3 to + 7,5 | V |
| Output voltage range (except FD, OA3) | $V_O$ | −0,3 to + 7,5 | V |
| Output voltage range (FD, OA3 only) | $V_O$ | −0,3 to + 15 | V |
| Output current (each output) | $I_O$ | max. 10 | mA |
| Operating ambient temperature range | $T_{amb}$ | −20 to + 70 | °C |
| Storage temperature range | $T_{stg}$ | −55 to + 125 | °C |

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## CHARACTERISTICS

$V_{SSA} = V_{SSD} = 0$ V; $T_{amb} = -20$ to + 70 °C unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **SUPPLIES** | | | | | |
| Supply voltage 1 (pin 28) | $V_{DD1}$ | 4,5 | 5,0 | 5,5 | V |
| Supply voltage 2 (pin 15) | $V_{DD2}$ | 10,8 | 12,0 | 13,2 | V |
| Back bias supply voltage (pin 1) | $-V_{BB}$ | 2,0 | 2,5 | 3,0 | V |
| Supply current 1 (pin 28) | $I_{DD1}$ | 30 | 60 | 150 | mA |
| Supply current 2 (pin 15) | $I_{DD2}$ | 4 | 8 | 21 | mA |
| Back bias supply current (pin 1) | $-I_{BB}$ | – | – | 500 | µA |
| **DIGITAL CIRCUITS** | | | | | |
| **Input HFD, $\overline{CRI}$** | | | | | |
| Input voltage LOW | $V_{IL}$ | −0,3 | – | + 0,8 | V |
| Input voltage HIGH | $V_{IH}$ | 2,4 | – | 6,5 | V |
| Input current (note 1) | $I_I$ | −1 | – | + 1 | µA |
| Input capacitance | $C_I$ | – | – | 7 | pF |
| **Outputs DADE/DEFM, $\overline{CLDE}$, FSDE, $\overline{SSDE}$, SBCL, SDATA, P, SWCL, $\overline{CEFM}$** (note 2) | | | | | |
| Output voltage LOW at $-I_{OL} = 1,6$ mA | $V_{OL}$ | 0 | – | 0,4 | V |
| Output voltage HIGH at $I_{OH} = 0,2$ mA | $V_{OH}$ | 3,0 | – | $V_{DD1}$ + 0,5 | V |
| Load capacitance | $C_L$ | – | – | 150 | pF |

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **DIGITAL CIRCUITS** (continued) | | | | | |
| **Output FD** | | | | | |
| Output voltage LOW at $-I_{OL} = 100\ \mu A$ | $V_{OL}$ | 0 | – | 0,5 | V |
| Output voltage HIGH at $I_{OH} = 100\ \mu A$ | $V_{OH}$ | 8,0 | – | $V_{DD2} + 0,5$ | V |
| Output leakage current at $V_O = 0$ to 6 V (note 3) | $\pm I_L$ | – | – | 1 | $\mu A$ |
| Output impedance | $Z_O$ | – | 1 | – | $k\Omega$ |
| **Outputs PD1, PD2** | | | | | |
| Output impedance | $Z_O$ | – | 5 | 10 | $k\Omega$ |
| **LEVEL DETECTOR** | | | | | |
| **Inputs HFI1, HFI2** | | | | | |
| A.C. input voltage range (peak-to-peak value) | $V_{I(p-p)}$ | 0,25 | – | 2,5 | V |
| Input capacitance | $C_I$ | – | – | 7 | pF |
| **Output FB** | | | | | |
| Output current at $V_{FB} = 2$ V | $I_{FB}$ | – | 150 | – | $\mu A$ |
| **OPERATIONAL AMPLIFIER** (note 4) | | | | | |
| **Inputs OA1, OA2** | | | | | |
| Common-mode voltage range | $V_{CIM}$ | 1,5 | – | 6,0 | V |
| Input offset voltage | $\pm V_{IOF}$ | – | 20 | – | mV |
| Input current (note 1) | $\pm I_I$ | – | – | 1 | $\mu A$ |
| Input offset current (note 5) | $\pm I_{IOF}$ | – | – | 0,1 | $\mu A$ |
| Input capacitance | $C_I$ | – | – | 7 | pF |
| Common-mode rejection ratio | CMRR | 40 | – | – | dB |
| Open loop gain (d.c.) | A | 40 | – | – | dB |
| Gain bandwidth product (20 dB/decade roll-off) | | 1 | 5 | – | MHz |
| **Output OA3** | | | | | |
| Output voltage LOW at $-I_{OL} = 1$ mA | $V_{OL}$ | 0 | – | 1 | V |
| Output voltage HIGH at $I_{OH} = 1$ mA | $V_{OH}$ | 8,0 | – | $V_{DD2} + 0,5$ | V |

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## CHARACTERISTICS (continued)

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **VCO** | | | | | |
| **Input VCO1, output VCO2** | | | | | |
| Mutual conductance at 100 kHz | $g_m$ | 1,5 | – | – | mA/V |
| Bandwidth (−3 dB cut-off) | $B_{gm}$ | 20 | – | – | MHz |
| Input capacitance | $C_I$ | – | – | 7 | pF |
| Output capacitance | $C_O$ | – | – | 7 | pF |
| Feedback capacitance | $C_{FB}$ | – | – | 5 | pF |
| Input leakage current (note 1) | $\pm I_I$ | – | – | 1 | μA |
| Output current at 10 MHz | $\pm I_O$ | – | 1 | – | mA |
| Small-signal voltage gain at 100 kHz | $A_V$ | 4 | – | – | V/V |
| **TIMING** | | | | | |
| Operating frequency (except VCO) | $F_{CEFM}$ | 0,1 | – | 5 | MHz |
| Operating frequency (VCO only) | $F_{VCO}$ | 0,2 | – | 10 | MHz |
| **Outputs $\overline{\text{CLDE}}$, DADE, $\overline{\text{SSDE}}$, FSDE, $\overline{\text{CEFM}}$** (Fig. 6 and note 6) | | | | | |
| Output rise time | $t_{OR}$ | – | – | 50 | ns |
| Output fall time | $t_{OF}$ | – | – | 40 | ns |
| $\overline{\text{CLDE}}$ period | $t_{OCP}$ | 400 | – | – | ns |
| $\overline{\text{CLDE}}$ HIGH time | $t_{OCH}$ | 150 | – | – | ns |
| $\overline{\text{CLDE}}$ LOW time | $t_{OCL}$ | 150 | – | – | ns |
| DADE/$\overline{\text{SSDE}}$/FSDE to $\overline{\text{CLDE}}$ set-up time | $t_{ODS}$ | 100 | – | – | ns |
| $\overline{\text{CLDE}}$ to DADE/$\overline{\text{SSDE}}$/FSDE hold time | $t_{ODH}$ | 100 | – | – | ns |
| $\overline{\text{SSDE}}$ LOW time (note 7) | $t_{SSL}$ | – | 3 | – | $\overline{\text{CEFM}}$ period |
| $\overline{\text{CLDE}}$ LOW time during FSDE (Fig. 5 and note 8) | $t_{OCG}$ | 16 | 46 | – | $\overline{\text{CEFM}}$ period |
| **Outputs SBCL, SDATA, P, SWCL** (Fig. 7) | | | | | |
| Output rise time (SBCL, SDATA) (note 6) | $t_{OR}$ | – | – | 50 | ns |
| Output fall time (SBCL, SDATA) (note 6) | $t_{OF}$ | – | – | 40 | ns |
| Output rise time (P, SWCL) (note 9) | $t_{OSR}$ | – | – | 200 | ns |
| Output fall time (P, SWCL) (note 9) | $t_{OSF}$ | – | – | 200 | ns |
| SBCL HIGH time | $t_{OCH}$ | 150 | – | – | ns |
| SBCL LOW time | $t_{OCL}$ | 150 | – | – | ns |
| SDATA to SBCL set-up time | $t_{ODS}$ | 100 | – | – | ns |
| P to SWCL set-up time | $t_{ODSP}$ | 1 | – | – | ns |
| SBCL to SDATA hold time | $t_{ODH}$ | 100 | – | 500 | ns |
| SBCL to SWCL hold time | $t_{SWH}$ | 0 | – | – | μs |
| SWCL duty cycle ($t_{HIGH}/t_{period}$) | | 40 | 50 | 60 | % |

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **TIMING** (continued) | | | | | |
| **Output FD** | | | | | |
| Output rise time (note 6) | $t_{FDR}$ | – | – | 1 | μs |
| Output fall time (note 6) | $t_{FDF}$ | – | – | 1 | μs |
| **Outputs DEFM, $\overline{CEFM}$** (Fig. 8) | | | | | |
| Output rise time (note 6) | $t_{OR}$ | – | – | 50 | ns |
| Output fall time (note 6) | $t_{OF}$ | – | – | 40 | ns |
| DEFM to $\overline{CEFM}$ set-up time (note 10) | $t_{ODS}$ | 50 | – | – | ns |
| $\overline{CEFM}$ to DEFM hold time (note 10) | $t_{ODH}$ | 70 | – | – | ns |
| $\overline{CEFM}$ HIGH time | $t_{OCH}$ | 50 | – | – | ns |
| $\overline{CEFM}$ LOW time | $t_{OCL}$ | 50 | – | – | ns |

## NOTES TO THE CHARACTERISTICS

1. At $T_{amb}$ = 25 °C; $V_{IN}$ = −0,3 to + 6,5 V; $V_{DD1}$ = 6,5 V.
2. Short-circuit protected to $V_{DD1}$ and $V_{SS}$. The maximum load capacitance that can be applied before short-circuit protection becomes operative is 150 pF.
3. At $T_{amb}$ = 25 °C; output in high impedance state.
4. All tests performed within common-mode voltage range.
5. At $T_{amb}$ = 25 °C.
6. Output loading = 50 pF.
7. $\overline{SSDE}$ remains LOW for only one negative edge of $\overline{CLDE}$.
8. Excessive bit-slip may cause gap to disappear. $\overline{CLDE}$ remains LOW when FSDE is HIGH.
9. Output loading = 150 pF.
10. Free running VCO frequency tuned to nominal and PLL in lock with a typical application circuit.

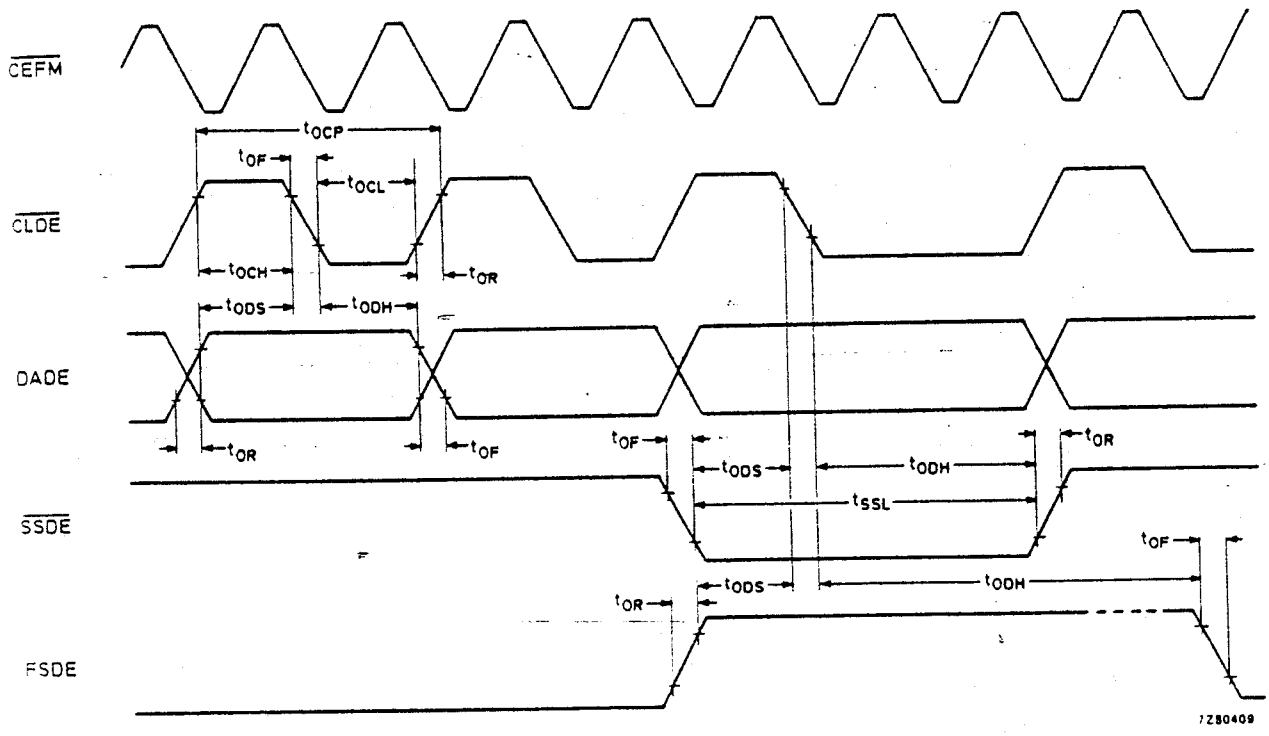


Fig. 6 Timing of waveform outputs to SAA7020.

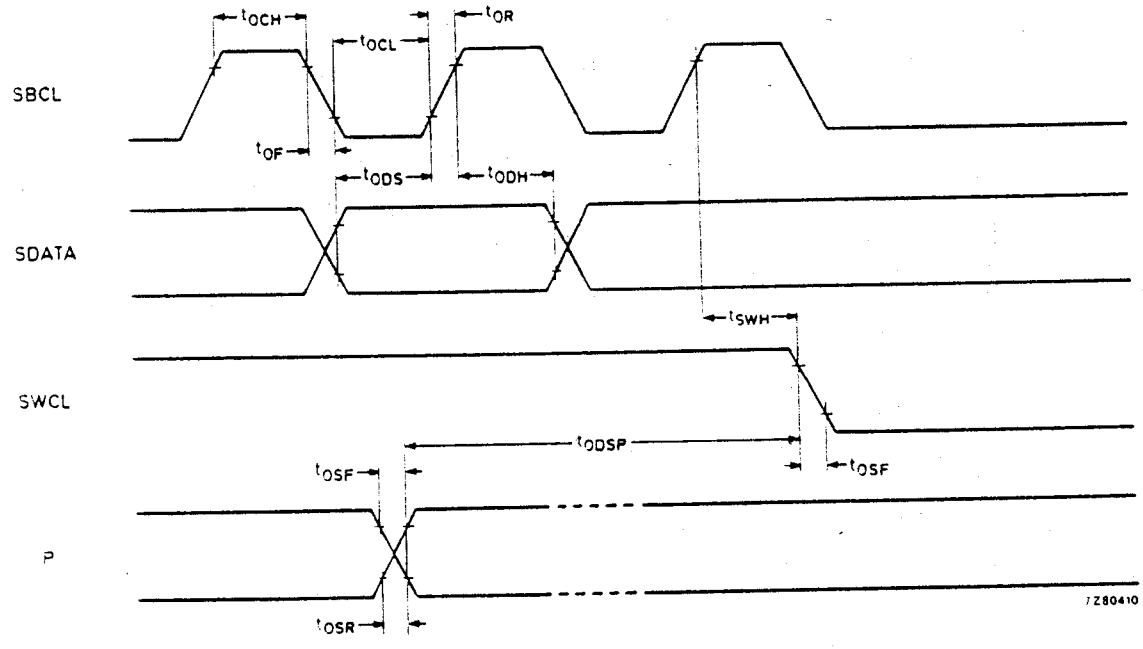


Fig. 7 Timing of waveform outputs for subcoding: reference levels are 0,8 and 2,4 V; SBCL and SDATA output loading = 50 pF; SWCL and P output loading = 150 pF; SWCL has a 50% duty cycle.

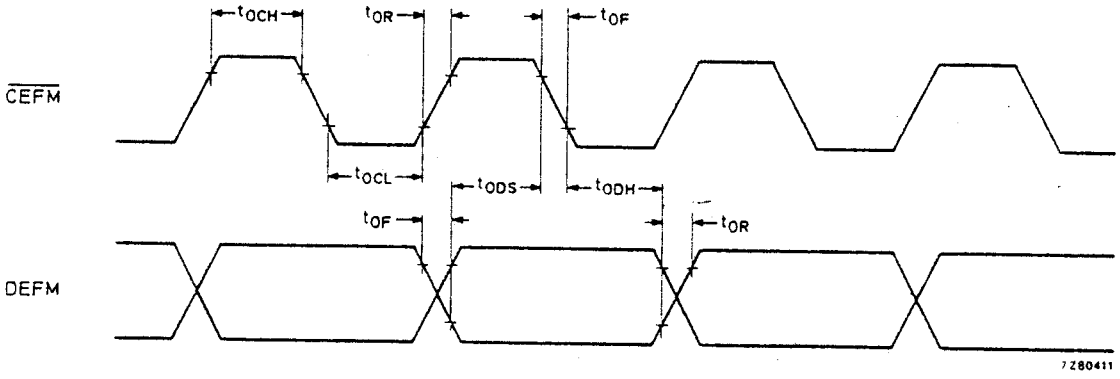


Fig. 8 Timing of EFM output waveforms: output loading = 50 pF; reference levels are 0,8 and 2,4 V.